REMARKS

The Examiner is thanked for his/her careful and very thorough Office Action. No claims are amended at this time. All rejections are hereby respectfully traversed. Favorable reconsideration of the claims is respectfully requested.

Rejection of Claims 1-5, 7-10, and 12-22 under 35 USC 103

Examiner has rejected all pending claims as obvious over Kaiser (EP publication number 0 766 177) in view of Blinn ("The Truth About Texture Mapping").

Claim 1 is reproduced for purposes of discussion:

> 1. A computer system, comprising:
>
> a graphics accelerator unit which manages page faulting of texture data invisibly to the host processor.

In rejecting claim 1, Examiner cites Kaiser at col. 3, line 50-col. 4, line 23, which states in part:

> It is an advantage of the present invention that 3D graphics processing may be efficiently accomplished by an auxiliary function processor in a controller connected to the processor bus, without the overhead of the processor translating the addresses in the command blocks to real addresses, and further calling OS routines to lock down these addresses in real memory so that they cannot be swapped out while they are being processed by the auxiliary function processor.

Though this passage says that the processor is relieved of the duty of "translating the addresses in the command blocks to real addresses," the passage goes on to say that OS (Operating System) routines are called to lock down the addresses in real memory. Though the Kaiser reference does not explicitly say this, OS routines are typically run by the host processor. Hence, calling OS routines to lock down the addresses in real memory fails to teach

the claimed limitation of, "a graphics accelerator unit which manages page faulting of texture data invisibly to the host processor." Because the host processor is invoked and must spend cycles (executing OS routines to lock down the data), the data access is not "invisible" to the host processor.

Kaiser explains its method in more detail at col. 6, generally between lines 3-29, reproduced in part below:

> Since memory controller 204 is not a processor, it cannot deal directly with a page fault. If a page fault condition occurs while graphics processor 206 is processing a command block from the main processor complex 12, an error status packet reflecting the page fault condition is passed to the processor 12 by memory controller 204. Processor software recognizes the fault condition and causes the faulting address to be rerun. When processor 12 encounters the same page fault condition, system software (outside the scope of the present invention) resolves the condition and passes control back to the graphics processor 206.

Hence, the host processor (element 12 in Kaiser's FIG. 2) is involved when a page fault occurs, and must (1) receive the fault condition from the memory controller; (2) recognize the fault condition; (3) cause the faulting address to be rerun; and, (4) when it encounters the same page fault condition again, the system software (presumably executed by the host processor) resolves the condition and passes control back to the graphics processor.

Further in the cited reference, Kaiser explains the central purpose of his patent, and the specific and limited functions that Kaiser teaches are offloaded from host processor. For example, Kaiser explains at col. 6, beginning at line 21:

> An additional mechanism is added to the address translation logic to handle synchronization of reference (R) and (C) bits in system page table 226. Normally, the R and C bits are updated by processor 12 and used by the software kernel to implement page casting algorithms. The

> graphics processor 206, however, does not update the R and C bits. This raises the possibility that a situation may arise where a page may be updated by graphics processor 206, but that same page has been invalidated by the software kernel resetting the C bit. To avoid such situations, the address translation logic checks the C bit in entries of page table buffer 226 to verify that the C bit is set for the matching entry in translation table? [sic] If the C bit is not set, the page fault mechanism described above is triggered.

[Emphasis added.]

Hence, though one task is in fact offloaded from the host processor of Kaiser (namely, updating the R and C bits), several other tasks are still performed by the host processor (as listed above), and new tasks are added (e.g., rerunning a faulted address of which it has been informed by the memory controller).

Hence, Applicant respectfully submits that the cited reference fails to teach or suggest the claimed limitations in at least claim 1.

The other independent claims are rejected under the rationale presented against claim 1. Hence, all other independent claims are believed distinguished from the cited references.

Because of their dependence on allowable claims, all dependent claims are therefore believed allowable.

Favorable reconsideration is respectfully requested.

Docket No.

Conclusion

Thus, all grounds of rejection and/or objection are traversed or accommodated, and favorable reconsideration and allowance are respectfully requested. The Examiner is requested to telephone the undersigned attorney or Robert Groover for an interview to resolve any remaining issues.

July 18, 2006

Respectfully submitted,

Patrick C. R. Holmes, Reg. No. 46,380
Attorney for Applicant

Customer Number 29106
Groover & Holmes
PO Box 802889
Dallas, TX 75380
Tel: 972-980-5840
fax: 972-980-5841